

Fig.1

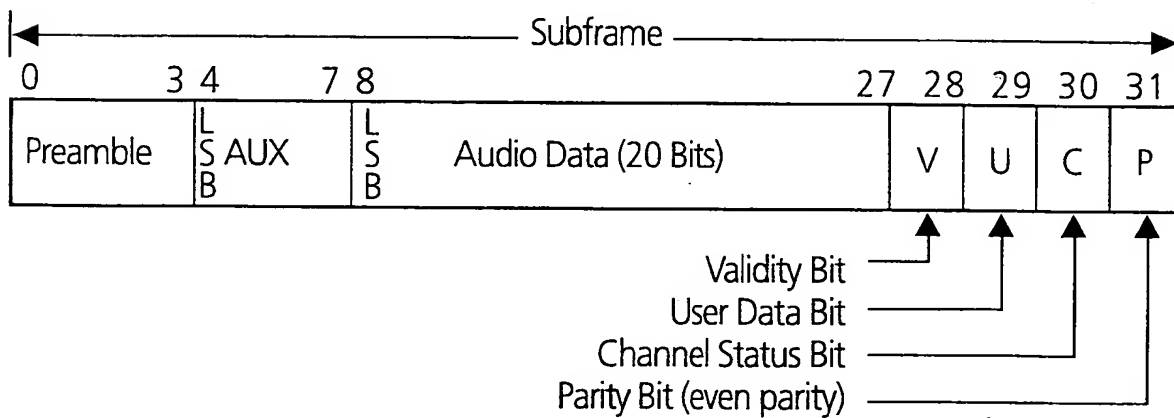


Fig.2

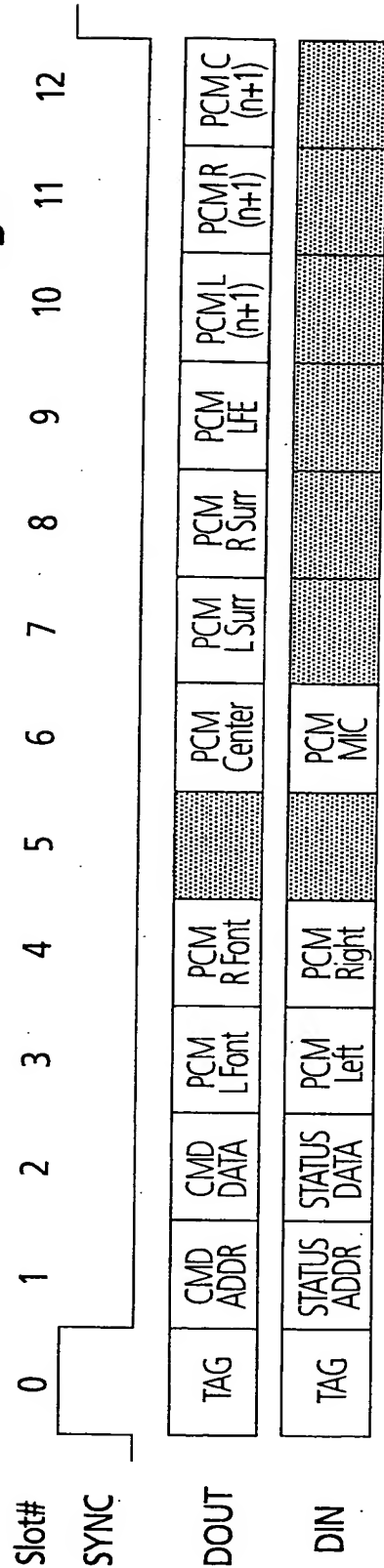
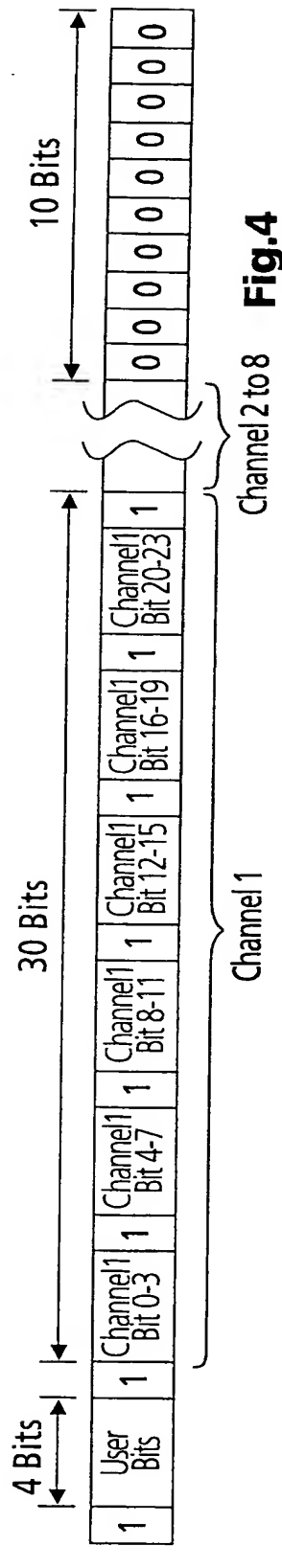


Fig. 3

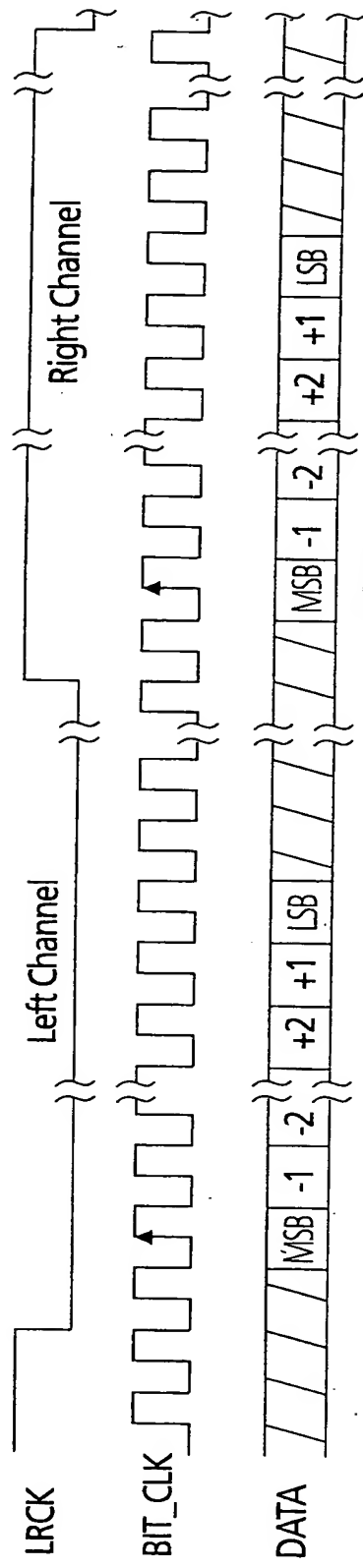


Fig. 5

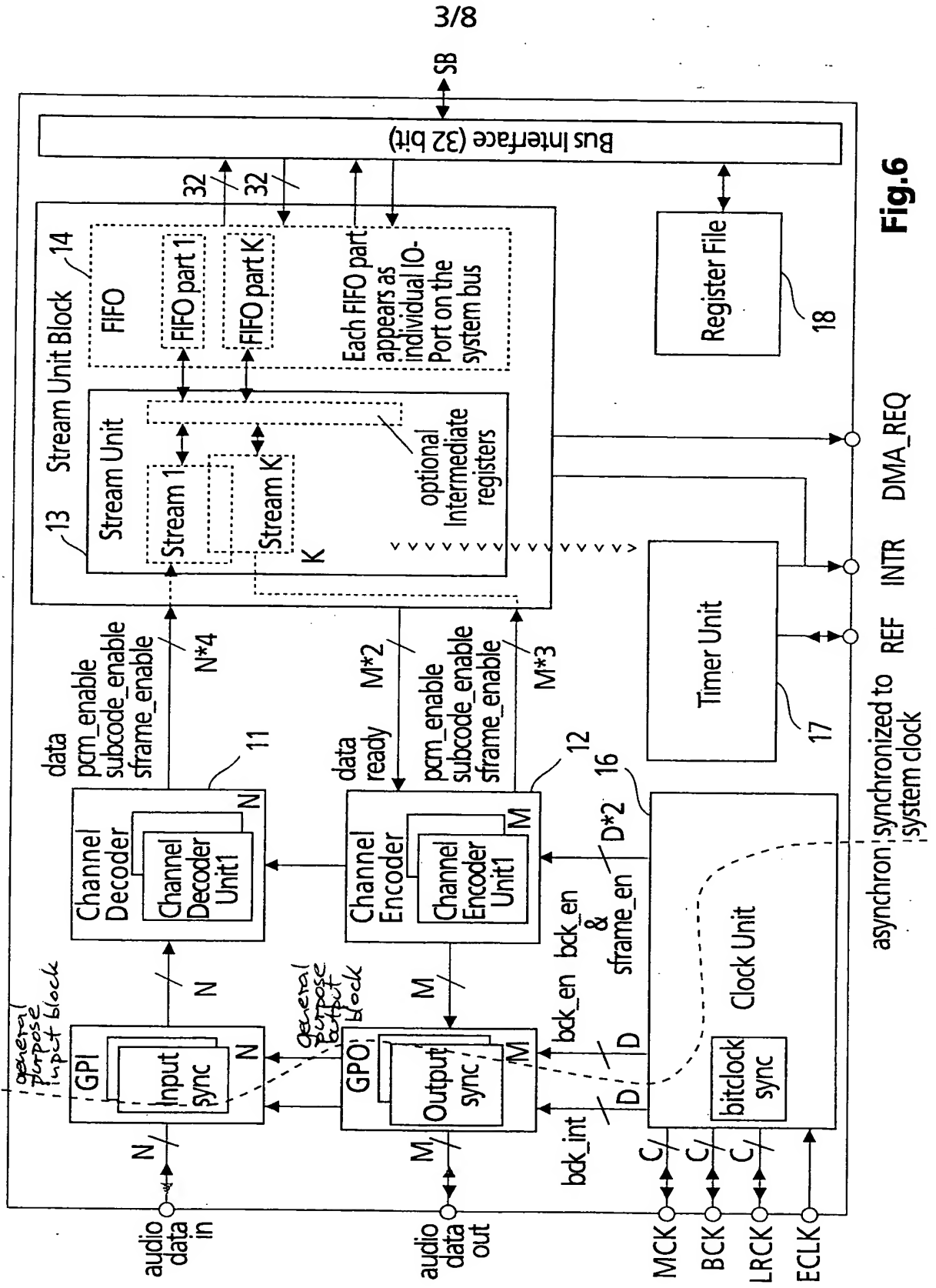


Fig.6

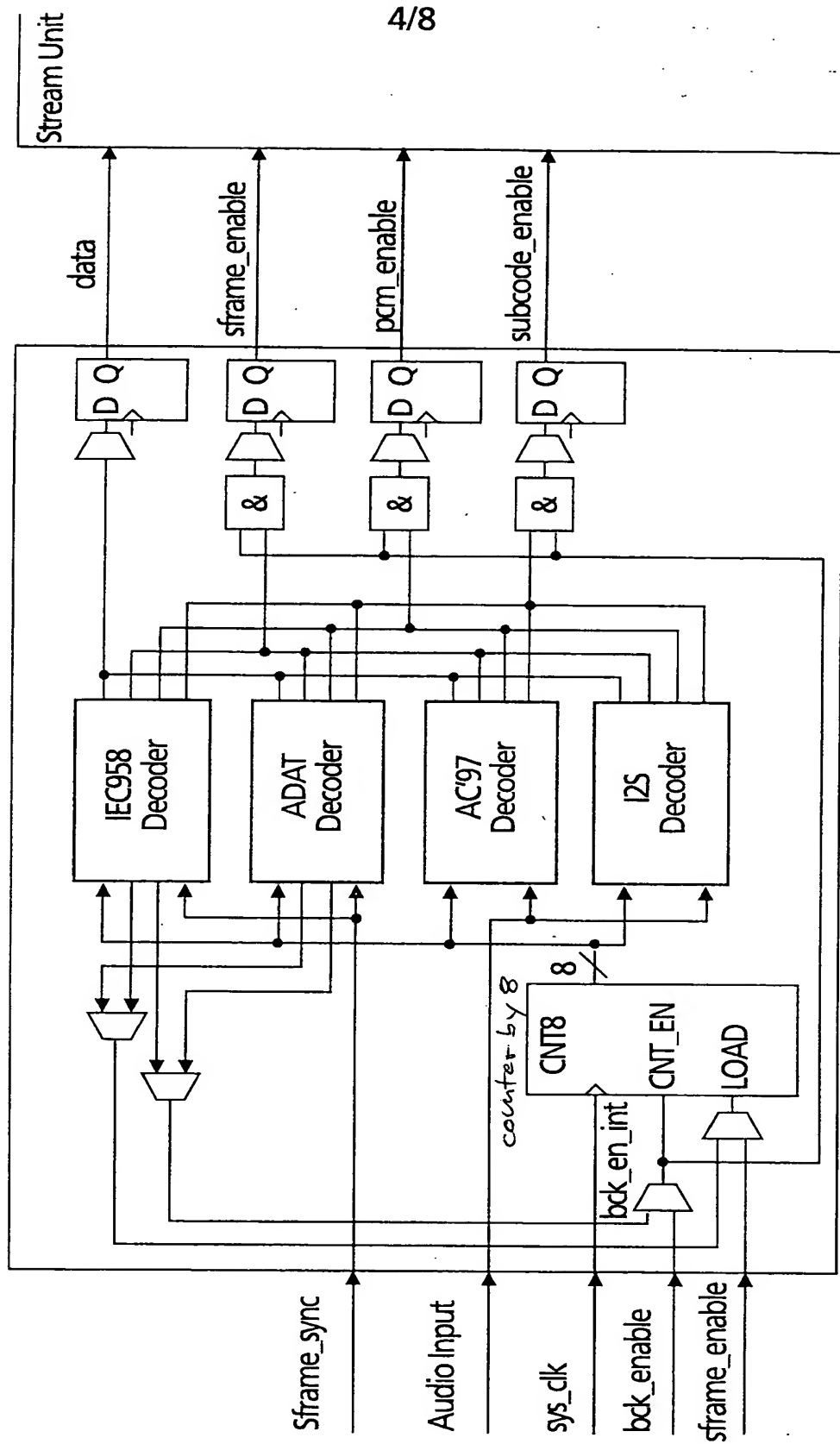


Fig.7

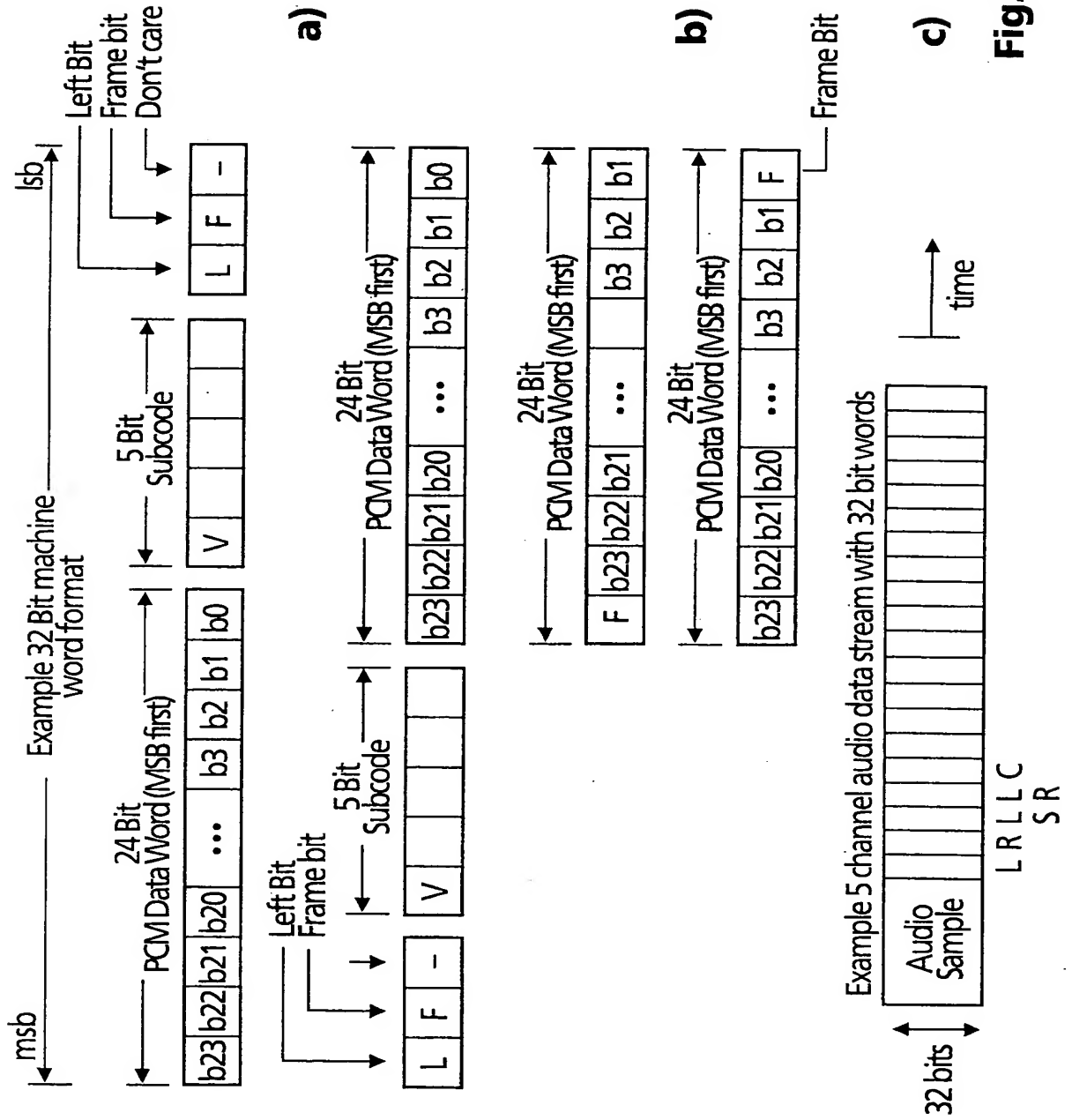


Fig.8

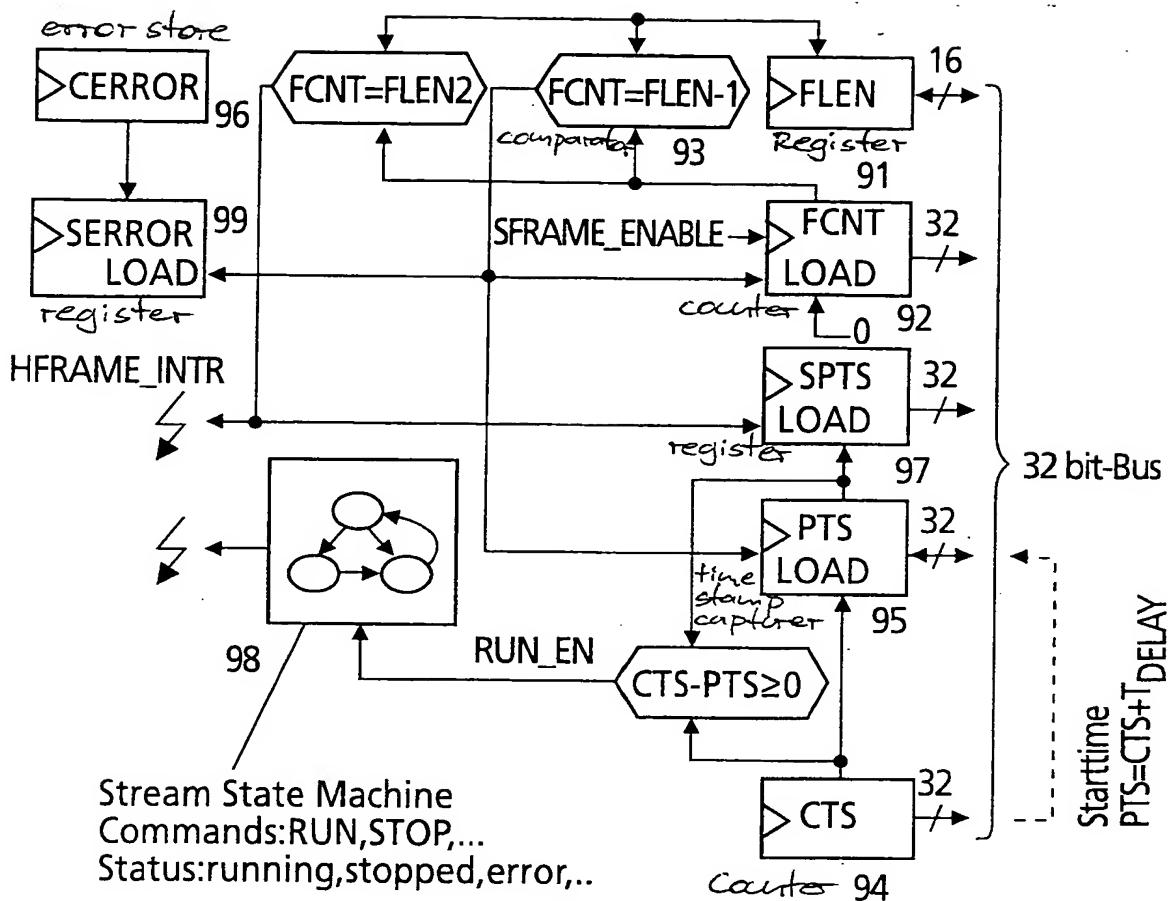


Fig.9

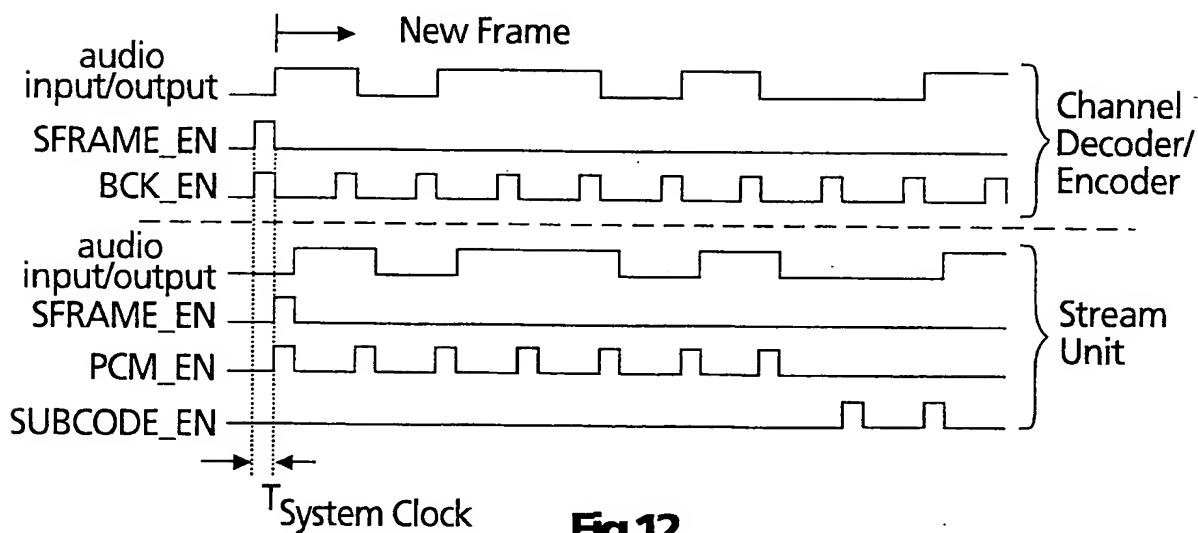


Fig.12

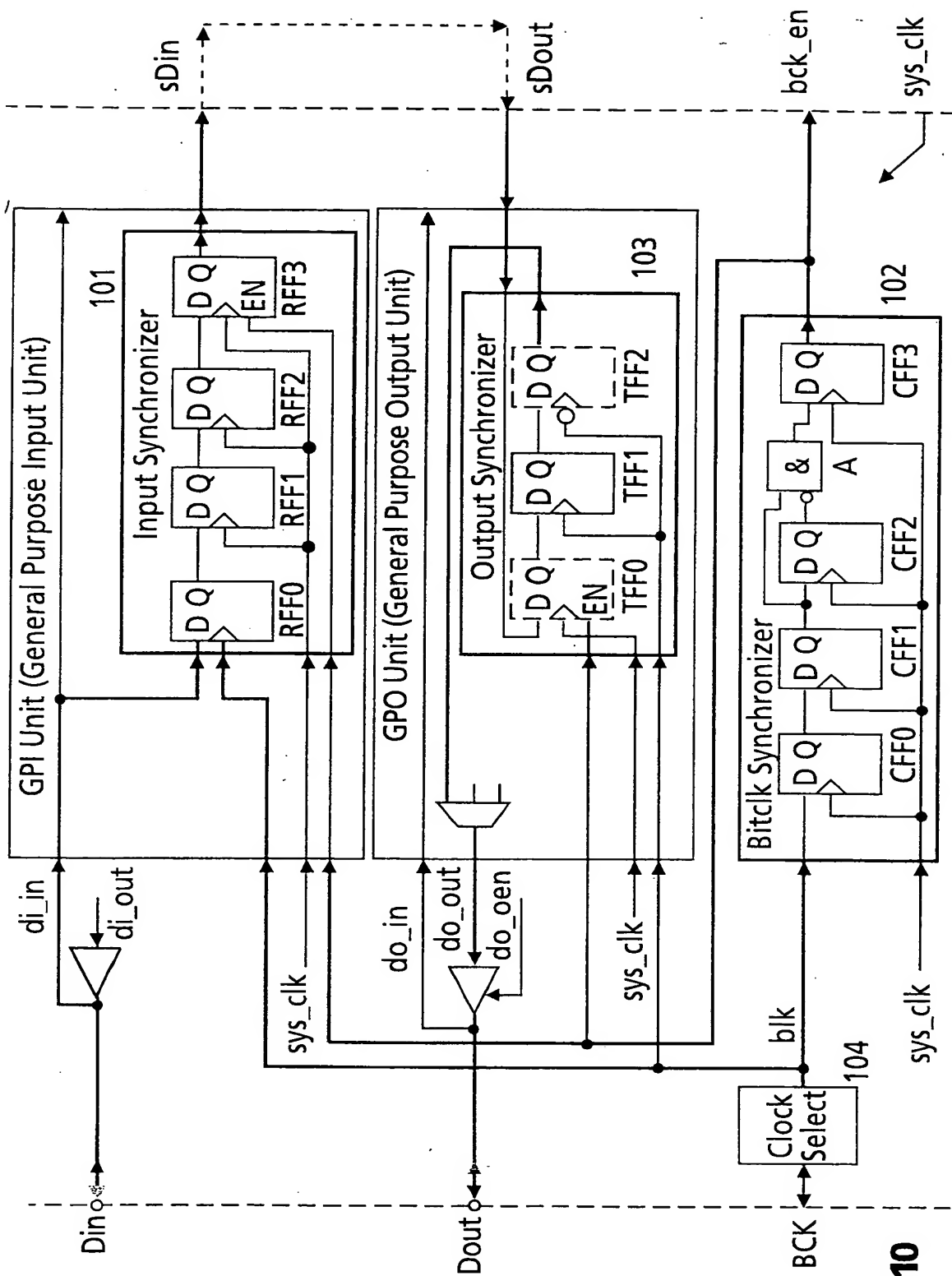
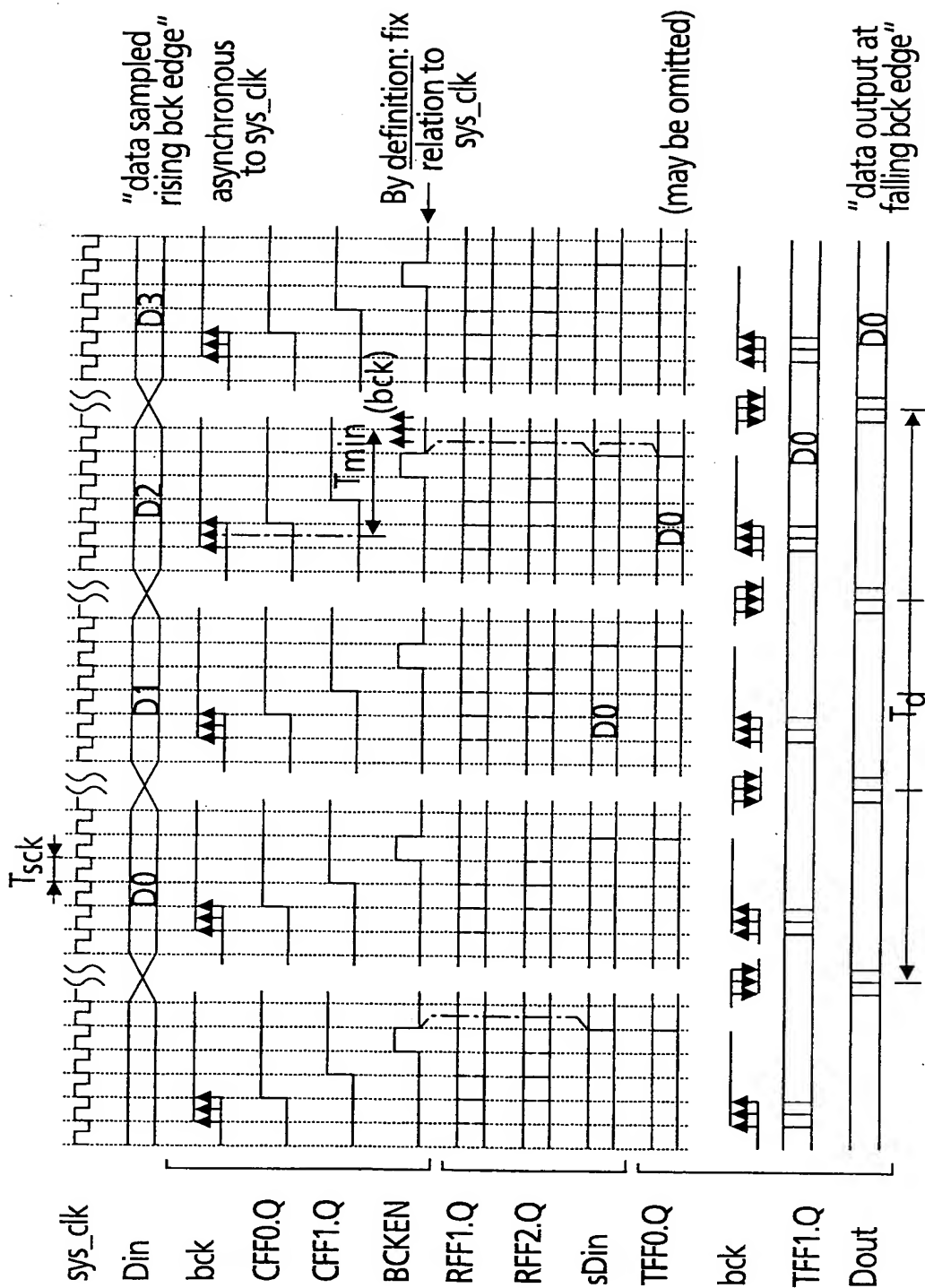


Fig.10



Constant Synchronizer Data delay: using opt. TFF0 : 3 bck cycles --if-- $T_{min} > 4 * T_{sck} + (T_{clkToOut} + T_{setup} + T_{safety})$ (i.e. $F_{sysclk} > (4.x) * F_{bck}$)
 without/bypassing: 2 bck cycles

Fig.11